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Gate-voltage dependence of low-frequency noise in GaN/AlGaN heterostructure field-effect transistors

A. Balandin

The gate-voltage dependence of low-frequency noise in GaN/AlGaN heterostructure field-effect transistors has been investigated in the linear and subsaturation regions. Analysis of experimental data for different transistors indicates that for all examined biases the noise spectrum is dominated by the channel noise rather than noise originating in the series resistors. The obtained results shed new light on the noise sources and may lead to improvements in the noise performance of GaN transistors.

Introduction: The low-frequency ($1/f^\gamma$) noise in GaN/AlGaN heterostructure field-effect transistors (HFETs) is currently attracting much attention (γ is a parameter close to 1). This is due to the demonstrated potential of GaN HFETs for high-power density and high frequency applications [1, 2], as well as to some unusual properties of $1/f^\gamma$ noise in these devices. The latter include a high noise spectral density, several order of magnitude differences in the Hooge parameter extracted for similar devices, large deviation of γ from 1, and strong dependence of γ on the applied gate bias. It also appears to be impossible to describe the noise in GaN/AlGaN HFETs with the models developed for conventional Si and GaAs devices [2 – 5]. Discrepancies in the data reported by different groups have prompted suggestions that the noise may be due in large part not to the device channels but to series resistors at the drain and source sides of the channel or to some ungated parasitic channels [6]. Taking into account the state-of-the-art quality of GaN material, this suggestion seems feasible. In this Letter I report results that may help to locate the dominant noise source in GaN HFETs.

Table 1: Parameters of GaN/AlGaN HFETs

Device	L_G	W	μ	n_s	Substrate
	μm	mm	cm^2V/s	cm^{-2}	
D	1.0	50 × 2	1339	0.9×10^{13}	SiC
C	1.0	50 × 2	616	1.1×10^{13}	SiC
E	0.25	40 × 2	460	1.5×10^{13}	sapphire
F	0.25	40 × 2	460	1.6×10^{13}	sapphire

Devices under test: One of the ways to distinguish different noise sources in a device under test is to study the gate voltage dependence of the relative drain current noise spectral density. The formalism developed by Peransin *et al.* [7] enables us to determine when the noise is dominated by the channel contribution, and when it is dominated by the excess noise coming from series resistances (poor contacts, etc.). Gate voltage dependence has also been used to distinguish between surface trapping noise and volume mobility fluctuation noise mechanisms [8]. The GaN HFET parameters selected for this study are summarised in Table 1. A detailed structure of these devices was given in [2]. The breakdown voltage for the devices is close to 80V. The channel conductance $G_{ch} = 1/R_{ch}$ is proportional to the effective gate voltage $V_G = V_{GS} - V_T$ in the linear region. The latter approximately holds even in the subsaturation region shown in Fig. 1.

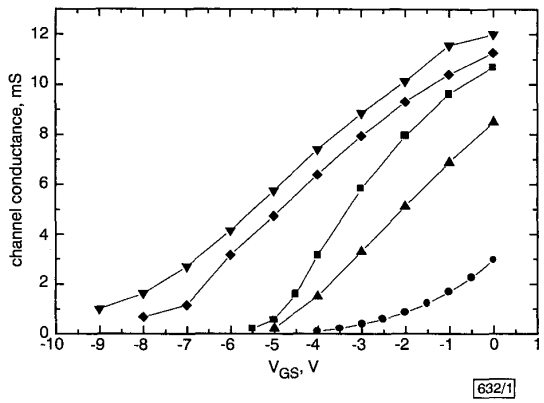

Fig. 1 *Channel conduction against gate voltage V_{GS} for different GaN HFETs in subsaturation region of operation (V_{DS} = 5.0 V)*

▲ D
● C
◆ E
■ F
▼ A

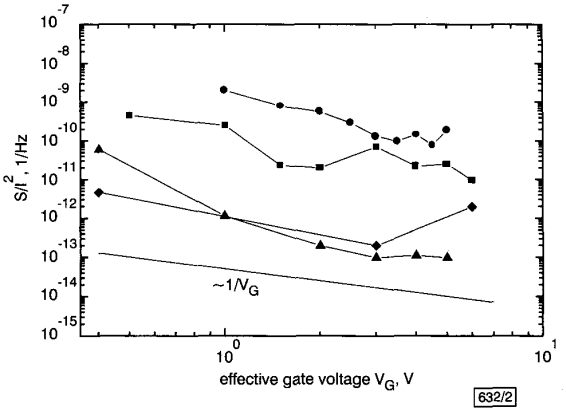

Fig. 2 *Drain-current noise spectral density against effective gate bias in linear region*

V_{DS} = 0.5V, f = 1.0kHz
▲ D
● C
◆ E
■ F
$1/V_G$ dependence is shown for comparison

Noise gate-bias dependence: Since the channel resistance R_{ch} is in series with the gate voltage independent resistors R_s, the total resistance between the source and drain is $R = R_{ch} + R_s$. Following the derivation in [7], the measured noise spectral density S_R for uncorrelated noise contributions can be written as

$$S_R = S_{R_{ch}} + S_{R_s} = \frac{\alpha_{ch} R_{ch}^2}{N_{ch} f} + S_{R_s} \simeq \frac{\alpha_{ch} e \mu R_{ch}^3}{L_{ch}^2 f} + S_{R_s} \quad (1)$$

where f is the frequency, e is the charge of an electron, μ is the mobility, L_{ch} is the channel length, $N_{ch} = L_{ch}^2/e\mu R_{ch}$ is the total number of carriers in the channel, and α_{ch} is the Hooge parameter. Since the first term in eqn. 1 is inversely proportional to V_G^3, and the second term does not depend on V_G, there are four possible gate-bias dependencies for the relative noise spectral density S_I/I^2. Some of them are stated below. If the resistance and noise are dominated by the channel of the device, e.g. $R_{ch} >> R_s$ and $S_{Rch} >> S_{Rs}$, then $S_I/I^2 = S_R/R^2 \simeq S_{Rch}/R_{ch}^2 \simeq 1/V_G$. If the total resistance is dominated by a series resistance but the noise mostly stems from the channel, then $S_I/I^2 = S_R/R^2 \simeq S_{Rch}/R_s^2 \simeq 1/V_G^3$. If both resistance and noise are dominated by the series resistance then, according to eqn. 1, there should be no V_G dependence. This analysis is rather general and can be applied to different FET and

HEMT-type devices, including GaN devices, since the only simplifications used were a homogeneous channel approximation and the Hooge empirical relation.

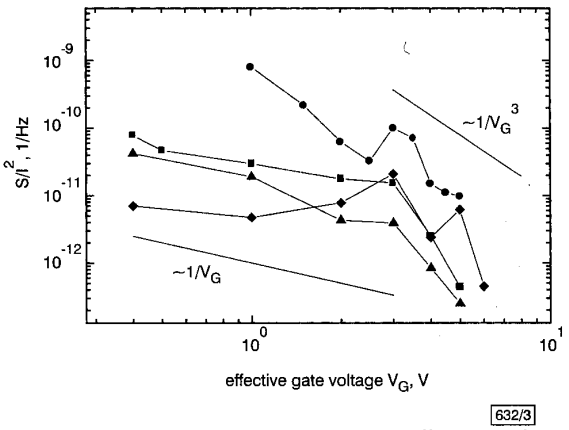

Fig. 3 *Drain-current noise spectral density against effective gate bias in subsaturation region*

V_{DS} = 5.0V, f = 1.0kHz
▲ D
● C
◆ E
■ F
$1/V_G$ and $1/V_G^3$ dependencies are shown for comparison

Experimental results: The low-frequency noise characteristics of GaN/AlGaN HFETs have been measured over a wide range of biasing conditions from the linear (V_{DS} = 0.5V) to subsaturation (V_{DS} = 5.0V) region. The measurements have been carried out using a low-noise amplifier with three stages, a dynamic signal analyser and bias power supplies [2, 5]. The noise spectral density in the frequency range 0.01–100kHz was determined to be of $1/f^{\gamma}$ type with γ varying from 1.0 to 1.3. The normalised drain current noise spectral density S_I/I^2 for fixed frequency f = 1.0kHz is shown in Figs. 2 and 3 as a function of the effective gate voltage in the linear and subsaturation regions, respectively. It can be clearly seen in Fig. 2 that in the examined range of biases, the noise spectral density is approximately inversely proportional to the effective gate bias. According to eqn. 1, it means that in the Ohmic regime the dominant noise contribution is from the device channel rather than from parasitic series resistors. In the subsaturation region (Fig. 3), the noise spectral density has two different regions characterised by the dependence $S_I/I^2 \simeq 1/V_G^m$, where m is close to 1 (for $V_G < 3$V), or is equal to or greater than 3. This still corresponds to the case when the dominant noise source is in the device channel. Some deviations from the gate-bias power laws derived from eqn. 1 can be traced back to the channel conductance dependence (see Fig. 1). Experimental errors may have also contributed to the discrepancy.

Conclusions: Experimental data, reported in this Letter, reveal that the noise spectral density in GaN/AlGaN HFETs is inversely proportional to the effective gate voltage over a wide range of biases. The presented quantitative analysis suggests that the dominant noise source is located in the device channel rather than in poor ohmic contacts or series resistors. This conclusion is important for obtaining further improvements in GaN/AlGaN transistor technology.

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Silicon planar ACCUFET: improved power MOSFET structure

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An improved power MOSFET structure in silicon, called the planar ACCUmulation channel field effect transistor (planar ACCUFET) is proposed. In this device, the P base and the deep P^+ regions of the conventional DMOSFET are replaced by a depleted N-type base region created using a buried P^+ region. Numerical simulations show that the planar ACCUFET has good forward blocking characteristics with low leakage current. The specific on-resistance, as well as the gate charge of the planar ACCUFET are lower than those of a DMOSFET with the same voltage rating. Furthermore, the planar ACCUFET requires a smaller thermal budget for fabrication than the DMOSFET.

Introduction: Power MOSFETs are the most popular power transistors for low voltage (< 200V) and high frequency switching applications [1]. Two important areas of improvement for the power MOSFET are the decrease in its conduction losses which are governed by its specific on-resistance ($R_{on,sp}$) and its switching losses which depend on its parasitic input capacitances. A number of alternate MOSFET structures with lower $R_{on,sp}$ have been proposed in the literature. These include the UMOSFET [2] which eliminates the parasitic JFET series resistance, and the COOLMOS [3] which employs charge compensation to increase the doping in the drift region. However, the tradeoffs in all these devices is either an increase in the switching losses due to an increase in the gate capacitance, or a significant increase in the complexity of the fabrication process as compared to that of the standard DMOSFET process, or both. A new power MOSFET structure called the planar ACCUFET was proposed [4] and realised in SiC [5]. In this Letter, we extend the work to silicon and show that the silicon planar ACCUFET has a lower specific on-resistance than that of a DMOSFET, without entailing any of the above mentioned tradeoffs.

Device structure and operation principle: Cross-sections of the proposed device and the DMOSFET are shown in Figs. 1*a* and *b*, respectively. In the planar ACCUFET, the P base region of the conventional inversion channel devices is replaced by a depleted N-type base region formed by the presence of a buried P^+ layer under the MOS gate. The depth of the buried P^+ region and the