

# Bias-Voltage Driven Switching of the Charge-Density-Wave and Normal Metallic Phases in 1T-TaS<sub>2</sub> Thin-Film Devices

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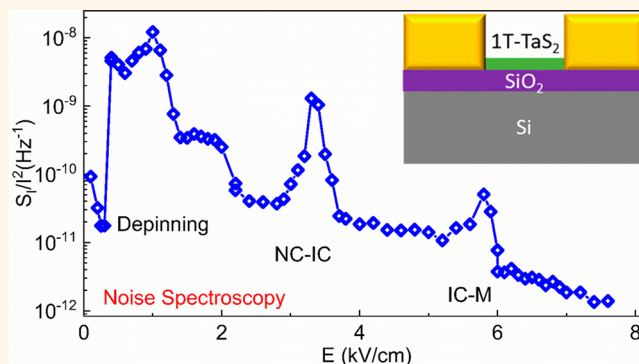
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## Supporting Information

**ABSTRACT:** We report on switching among three charge-density-wave phases, commensurate, nearly commensurate, incommensurate, and the high-temperature normal metallic phase in thin-film 1T-TaS<sub>2</sub> devices induced by application of an in-plane bias voltage. The switching among all phases has been achieved over a wide temperature range, from 77 to 400 K. The low-frequency electronic noise spectroscopy has been used as an effective tool for monitoring the transitions, particularly the switching from the incommensurate charge-density-wave phase to the normal metal phase. The noise spectral density exhibits sharp increases at the phase transition points, which correspond to the step-like changes in resistivity. Assignment of the phases is consistent with low-field resistivity measurements over the temperature range from 77 to 600 K. Analysis of the experimental data and calculations of heat dissipation indicate that Joule heating plays a dominant role in the voltage induced transitions in the 1T-TaS<sub>2</sub> devices on Si/SiO<sub>2</sub> substrates, contrary to some recent claims. The possibility of the bias-voltage switching among four different phases of 1T-TaS<sub>2</sub> is a promising step toward nanoscale device applications. The results also demonstrate the potential of noise spectroscopy for investigating and identifying phase transitions in the materials.

**KEYWORDS:** charge-density-wave effects, van der Waals materials, voltage switching, resistive switching, low-frequency noise, 1T-TaS<sub>2</sub>, normal metallic phase, Joule heating



Switching between various material phases at room temperature by the application of bias voltage has the potential of becoming a new device paradigm for future electronic and optoelectronic technologies.<sup>1–4</sup> Among the promising material candidates, which exhibit phase changes characterized by abrupt resistivity changes and hysteresis, is the 1T polymorph of tantalum disulfide (TaS<sub>2</sub>). The quasi-two-dimensional (2D) van der Waals layered crystalline 1T-TaS<sub>2</sub> exhibits charge-density-wave (CDW) effects, that is, periodic modulation of the charge density and the underlying lattice resulting from the interplay between the electron–electron and electron–phonon interactions.<sup>5–14</sup> The CDW state becomes fully commensurate with the lattice below ~200 K.<sup>15–17</sup> The

commensurate CDW (C-CDW) consists of a  $\sqrt{13} \times \sqrt{13}$  reconstruction within the basal plane that forms a star-of-David pattern in which each star contains 13 Ta atoms. The Fermi surface, composed of 1 *d*-electron per star, is unstable so that the lattice reconstruction is accompanied by a Mott-Hubbard transition that fully gaps the Fermi surface and increases the resistance.<sup>15,18–21</sup> As the temperature increases above 180 K, the C-CDW phase breaks up into a nearly commensurate

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CDW (NC-CDW) phase that consists of ordered C-CDW regions separated by domain walls.<sup>22</sup> This C-CDW to NC-CDW transition is revealed as an abrupt change in the resistance with a large hysteresis window in the resistance profile at  $\sim 200$  K. As the temperature is increased to  $\sim 350$  K, the NC-CDW phase melts into an incommensurate CDW (I-CDW) in which the CDW wave vector is no longer commensurate with the lattice. This transition is accompanied by a smaller hysteresis window in the resistivity.<sup>23,24</sup> Only at high temperatures of  $\sim 500$ – $600$  K does the I-CDW phase melt into the metallic normal phase (NP) of 1T-TaS<sub>2</sub>.<sup>5</sup> Until now, the transition from the I-CDW to the NP phases has been achieved only via heating of 1T-TaS<sub>2</sub> samples.

Apart from temperature, various CDW phase transitions in 1T-TaS<sub>2</sub> and some related materials, for example, 1T-TaSe<sub>2</sub>, can be induced by external perturbations including doping,<sup>7,17,25–30</sup> photoexcitation,<sup>8,31</sup> pressure,<sup>5</sup> carrier injection,<sup>6,32</sup> reduction of thickness,<sup>33–35</sup> electric field,<sup>9,24,32</sup> laser pulse,<sup>8,36</sup> and gate voltages.<sup>32,37,38</sup> The existence of several CDW phases, in addition to electrically driven switching among them within a short time scale, makes 1T-TaS<sub>2</sub> a particularly promising candidate for electronic device applications,<sup>6,32,39</sup> even though the exact nature of these phases continues to be a subject of debate.<sup>40–43</sup> Major impetus for this research came from the demonstration of a 1T-TaS<sub>2</sub>-based voltage controlled oscillator operating at room temperature (RT); this device utilizes the NC-CDW–I-CDW phase transition, which occurs at 350 K in the “low-bias” regime.<sup>37</sup> Here we refer to the resistivity as “low-bias” when it is measured at very low electric bias, that is, few mV, to guarantee the absence of self-heating and thus, preclude transitions induced entirely by the temperature change.<sup>37,44</sup> Subsequent work has focused on the implementation of such CDW devices for information processing and radiation-hard applications.<sup>45–48</sup> It has been demonstrated that such devices can be fast, low-power, and immune to proton and X-ray radiation.<sup>48</sup>

It has been suggested that electric field and current not only interact with the CDW but also result in Joule heating, which in turn causes the phase transitions in 1T-TaS<sub>2</sub>.<sup>49</sup> The extent to which the electrical field by itself, versus self-heating associated with the current conduction, is responsible for inducing transitions between C-CDW and NC-CDW or NC-CDW and I-CDW is still under intense debate.<sup>37,49,50</sup> Moreover, although the electric field induced C-CDW to NC-CDW and NC-CDW to I-CDW phase transitions in 1T-TaS<sub>2</sub> have been reported by many groups,<sup>6,37,51</sup> there have been no reports on the electric-field induced transition to the normal metallic phase. This situation can be attributed to the difficulty of reaching temperatures of  $T = 550$ – $600$  K via self-heating due to the applied electric bias and the less pronounced change in the resistivity at the I-CDW–normal phase (NP) transition. The possibility of using the I-CDW–NP transition for devices is attractive due to their anticipated radiation-hardness,<sup>47,48</sup> which stems from the inherent tolerance of metallic materials to radiation damage compared with semiconductors.

Here, we report on the I-CDW–NP transition induced by electrical bias in 1T-TaS<sub>2</sub> devices on conventional Si/SiO<sub>2</sub> wafers, operating over a wide temperature range. The measurements of the low-frequency electronic noise, that is, current fluctuations, have been used to unambiguously observe the phase transitions, particularly the switching from the I-CDW to NP. The low-frequency noise, typically with the

spectral density  $S(f) \approx 1/f^\gamma$  ( $f$  is the frequency and parameter  $\gamma \approx 1$ ), is found in almost all materials and devices.<sup>52,53</sup>

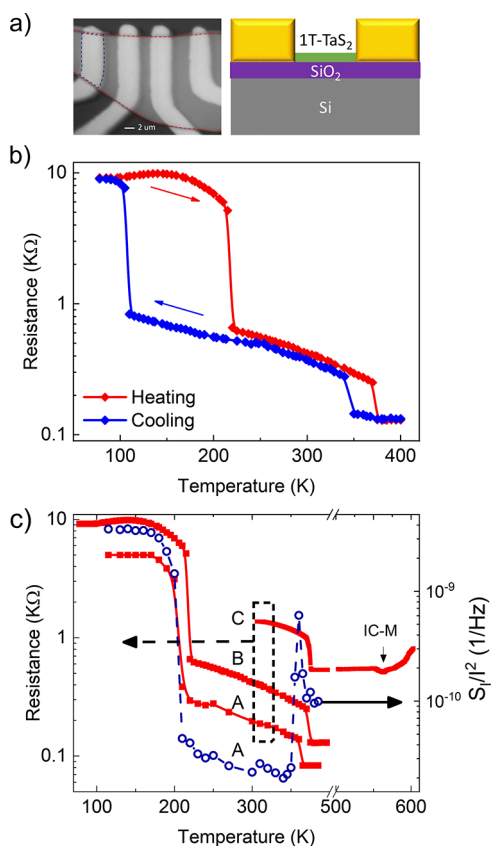
Although practical applications can benefit from the reduction of the low-frequency noise, it also can be used as a characterization tool that reveals information about the physical processes in materials.<sup>43,44,54,55</sup> The bias-voltage induced switching among three CDW phases and one normal phase of 1T-TaS<sub>2</sub> is demonstrated with the help of low-frequency-noise spectroscopy. The rest of the paper is organized as follows. First, the material preparation, device fabrication, and resistivity measurements are briefly outlined. Second, low-frequency noise measurements are described in the context of monitoring phase transitions and carrier transport in CDW materials. Third, simulation of heat dissipation is used to assess the relative importance of the self-heating and electric field for inducing CDW and metallic phase transitions.

## DEVICE FABRICATION AND MEASUREMENTS

Multimillimeter-sized crystals of 1T-TaS<sub>2</sub> were synthesized by iodine-mediated chemical vapor transport (CVT) (Methods), and their quality was evaluated by X-ray diffraction, energy dispersive spectroscopy, and Raman spectroscopy (Supporting Information). All results were in excellent agreement with reference data as previously detailed.<sup>38,45</sup> Thin layers of crystalline 1T-TaS<sub>2</sub> were cleaved by mechanical exfoliation and transferred to SiO<sub>2</sub>/Si substrates. We intentionally used 1T-TaS<sub>2</sub> layers with thicknesses greater than 9 nm to preserve the C-CDW–NC-CDW phase transition. It is known that 1T-TaS<sub>2</sub> quasi-2D films with thicknesses approaching a monolayer do not reveal the C-CDW–NC-CDW transition.<sup>23,37</sup> The transmission line measurement (TLM) pattern was used for device fabrication. The metal Ti/Au contacts were evaporated through a shadow mask to avoid chemical contamination and oxidation during the fabrication process. After the contact evaporation, the devices were transferred to another vacuum chamber for the transport measurement. Multiple 1T-TaS<sub>2</sub> devices were fabricated and tested. For the typical devices used in the study, the thickness was in the range from 25 to 100 nm, while the channel length was from 1 to 15  $\mu\text{m}$ . An optical microscopy image of a representative device together with the schematic of its layered structure are shown in Figure 1a. Additional microscopy images of tested devices with the 60 nm thick and 2- $\mu\text{m}$ -long 1T-TaS<sub>2</sub> channel can be seen in the Supporting Information. All current–voltage ( $I$ – $V$ ) characteristics and resistivities were measured in the cryogenic probe station (Lakeshore TTPX) with a semiconductor analyzer (Agilent B1500). The low-frequency noise experiments were conducted in the two-terminal device configuration but with different channel lengths. The noise spectra were measured with a dynamic signal analyzer (Stanford Research 785). Additional device fabrication details are provided in the Methods and Supporting Information.

## RESULTS AND DISCUSSION

Figure 1b shows resistance as a function of temperature for both cooling and heating cycles for a representative 1T-TaS<sub>2</sub> device with a channel thickness of  $H = 60$  nm. The data reveal two hysteresis windows at the C-CDW–NC-CDW phase transition ( $T = 200$  K) and NC-CDW–I-CDW phase transition ( $T = 355$  K), in line with previous reports.<sup>5</sup> The well-resolved hysteresis windows and their temperature ranges



**Figure 1.** (a) Optical image of a representative device (left panel) and a schematic of the device layered structure (right panel). The red and blue dashed lines show the contours of the 1T-TaS<sub>2</sub> channel and a metal contact, respectively. The scale bar is 2 μm. (b) Resistance as a function of temperature for cooling (blue curve) and heating (red curve) cycles conducted at the rate of 2 K per minute. The resistance reveals two characteristic hysteresis windows at the commensurate–nearly commensurate CDW transition at  $T \approx 200$  K and at the nearly commensurate–incommensurate CDW transition at  $T \approx 355$  K. (c) Resistance (red curves) and normalized noise spectral density (blue curve), as a function of temperature, measured in the heating cycle. The resistance is presented for three different 1T-TaS<sub>2</sub> devices (marked A, B, C). The noise spectral density, measured at  $f = 10$  Hz, is for device A. The device C was tested for higher temperatures to resolve the transition from incommensurate CDW to the normal metallic phase ( $T \approx 550$  K), marked as IC-M in the legend. All three devices show an abrupt resistance change at  $T \approx 355$  K due to the transition from nearly commensurate to incommensurate CDW phase. Two devices A and B, tested at low temperature, show an abrupt resistance change at  $T \approx 200$  K due to the transition from the commensurate to nearly commensurate CDW phase.

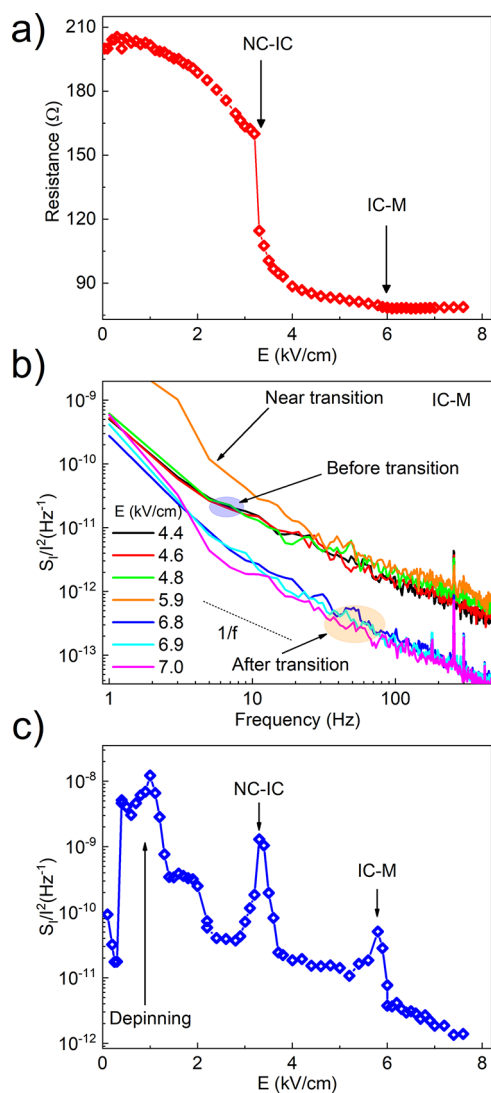
attest to the high-quality of the fabricated devices. In Figure 1c, we present resistance in the heating cycle in a wider temperature range (red curves) and normalized noise spectral density,  $S_I/I^2$ , at  $f = 11$  Hz (blue curves) as the functions of temperature ( $I$  is the current through the two-terminal device). The resistance is presented for three different 1T-TaS<sub>2</sub> devices (marked A, B, and C) to illustrate the reproducibility. The resistance and noise spectral density were measured at temperatures changing from low to high, with the heating rate of 2 K/min. The resistance and noise spectral density experience abrupt changes at the expected phase transition of 1T-TaS<sub>2</sub>, that is, C-CDW–NC-CDW near 200 K, NC-CDW–

I-CDW near 350 K, and, finally, I-CDW–NP near 550 K. Note that the NP (normal phase) and M (metallic) symbols and terminology are used interchangeably in the text and figures.

The noise level decreases by two orders of magnitude, from  $4 \times 10^{-9}$  Hz<sup>-1</sup> to  $4 \times 10^{-11}$  Hz<sup>-1</sup>, at the C-CDW–NC-CDW phase transition near 200 K, and it reveals a sharp, one order-of-magnitude peak at the NC-CDW–I-CDW phase transition near 350 K. The fact that we clearly observe the C-CDW–NC-CDW transition indicates that the selected 1T-TaS<sub>2</sub> thickness range is appropriate.<sup>23,37</sup> The abrupt changes in the noise spectral density happen at the same temperatures as the corresponding steps in the electrical resistance. Additional data confirming this conclusion are presented in the Supporting Information. Our measurements in the low-bias regime prove that the noise spectroscopy can be used as an efficient tool for monitoring the phase transitions in a 1T-TaS<sub>2</sub> device.<sup>44</sup>

Irrespective of the exact physical mechanism of the phase transitions in thin films of 1T-TaS<sub>2</sub>, that is, pure electric field effect, Joule self-heating or both, the electrical bias,  $V_T$ , required to induce the transitions should depend on the device geometry and design details. To induce the I-CDW–NP transition by the electric field, at reasonably low  $V_T$ , we fabricated devices with different geometries, channel lengths, and thicknesses. The strength of the applied field was varied from low to high (up to 35 kV/cm). The  $I$ – $V$  characteristics and noise spectral density were measured as the functions of the electric field at different temperatures. Figure 2 shows the resistance and noise characteristics of a 1T-TaS<sub>2</sub> device with 60 nm-thick channel, measured at RT. The resistance as a function of the applied electric field,  $E$ , is presented in Figure 2a. It drops sharply at the field of 3.6 kV/cm, which corresponds to the NC-CDW–I-CDW phase transition. At  $E = 6$  kV/cm, there is another relatively small step-like decrease in the resistance suggesting the I-CDW–NP transition. Although the change in the resistance is small, it is reproducible.

The normalized current noise spectral density,  $S_I/I^2$ , near the I-CDW–NP transition, is shown in Figure 2b. The data are presented for different values of the electric field. Away from the phase-transition field, the noise spectra are of  $1/f^\gamma$  type ( $\gamma \approx 1$ ), indicating that there were no electromigration or dominant defect states, that is, trap levels, with characteristic time constants.<sup>52,53</sup> The noise increases with the trace of a Lorentzian peak at the transition bias, which corresponds to the onset of the I-CDW–NP transition. The evolution of the noise spectral density over the entire range of electric bias can be seen in Figure 2c, which shows  $S_I/I^2$  ( $f = 10$  Hz) as a function of electric field. There are three abrupt noise peaks. The peaks at  $E = 3.6$  kV/cm and  $E = 6$  kV/cm correspond to the NC-CDW–I-CDW and I-CDW–NP transitions, respectively. The noise level increases near or at the phase transition points owing to the lattice reconstruction. One should note that noise peak at the transition to the normal phase is much more clear than the slight step in the resistance at the same value of the electric field. The latter proves the usefulness of the noise spectroscopy for monitoring phase transitions. There is another peak in the noise spectral density at the applied field  $E \approx 1$  kV/cm. We attribute this peak to the onset of CDW depinning, in line with our previous finding.<sup>44</sup> We also note that for some devices, the electric field to induce the phase transition, determined from the noise measurements, was somewhat lower than that from  $I$ – $V$  characteristics. This difference can be attributed to the differences in sweep rates



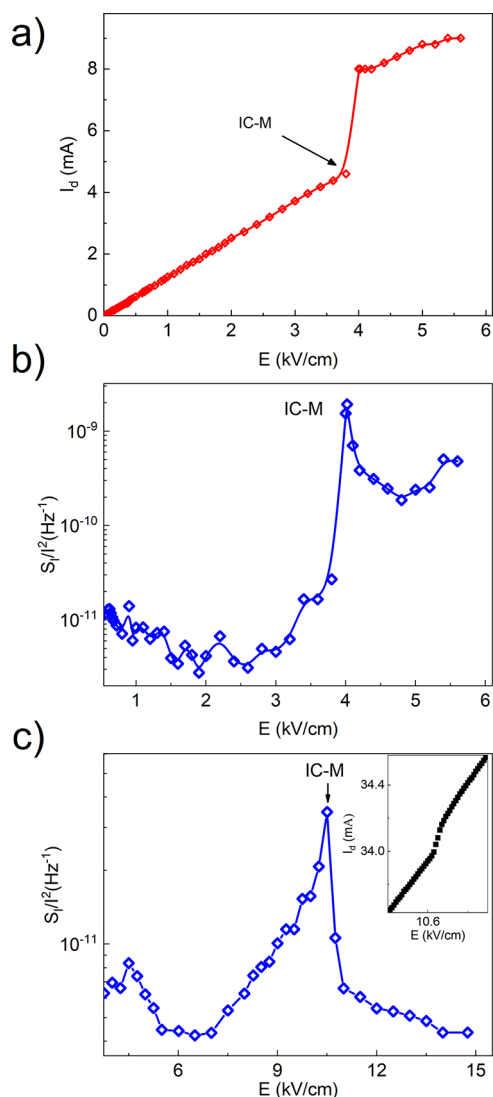
**Figure 2.** (a) Resistance as a function of the applied electric field for 1T-TaS<sub>2</sub> device measured at room temperature. The resistance drops sharply at  $E = 3.6$  kV/cm owing to the nearly commensurate to incommensurate CDW phase transition, marked as NC-IC in the legend. The slight step in resistance at  $E = 6.0$  kV/cm corresponds to the transition from incommensurate CDW phase to the normal metallic phase, marked as IC-M in the legend. (b) Normalized current noise spectral density as the function of frequency for several values of the electric field, which include the point of transition from the incommensurate CDW to the normal metallic phase. The noise level is the lowest in the metallic phase. It increases strongly at the electric field value, close to the one required for inducing the transition to the metallic state. (c) Normalized current noise spectral density, measured at  $f = 10$  Hz, as the function of the electric field. One can clearly see two peaks, which correspond to the NC-IC and IC-M phase transitions at  $E = 3.6$  kV/cm and  $E = 6.0$  kV/cm, respectively. An additional peak at  $E \approx 1.0$  kV/cm is attributed to the depinning of the charge density wave.

utilized for the  $I$ - $V$  and noise measurements. This conclusion is in agreement with literature reports, which found a dependence of the NC-CDW-I-CDW transition on the voltage sweep rate.<sup>49,56</sup> Additional details supporting our conclusions, as well as data for different devices, are provided in the Supporting Information.

To investigate in detail the I-CDW-NP transition specifically, several 1T-TaS<sub>2</sub> devices were heated to 400 K, which is well above the NC-CDW-I-CDW phase transition temperature but substantially below the I-CDW-NP transition temperature of 550 K (see resistance data for device C in Figure 1). The tested devices had different channel lengths and widths to alter the electric bias,  $V_B$ , needed to induce the I-CDW-NP transition either through the field strength or Joule heating. The evolution of electric current through the device and the normalized noise spectra density in one of the devices are shown in Figure 3a and b, respectively. The transition to metal phase is clearly seen as the step-like jump in the current,  $I$ , resistance,  $R = V_B/I$ , and as the peak in the normalized noise spectral density  $S_I/I^2$ . In this specific device, with larger dimensions, an electric field  $E \approx 10.6$  kV/cm is required to induce the transition to the metallic state. Note a pronounced noise peak at this value of the electric field, which exactly corresponds to the field of the jump in current to a lower resistivity state (see inset to Figure 3c). In other devices, the changes in the current were small, and the I-CDW-NP transition could be unambiguously determined only from the peak in the noise spectral density (see Figure 3c).

A possibility of the voltage-induced switching a CDW device to multiple resistive states by application of a small electric bias, for example, below 3 V at RT, is important for information processing and memory applications.<sup>57,58</sup> To demonstrate switching among all three CDW phases and one normal phase, we set the 1T-TaS<sub>2</sub> device to the C-CDW state by cooling it below 200 K. In a device with properly selected dimensions, the application of a relatively small electric bias can induce all three transitions. Figure 4a shows current as a function of the applied in-plane electric field at  $T = 77$  K. The current shows three consecutive hysteresis windows at the electric fields of 25.0 kV/cm, 31.3 kV/cm, and 32.1 kV/cm, which correspond to the C-CDW-NC-CDW, NC-CDW-I-CDW, and I-CDW-NP transitions, respectively. The voltage-induced resistive switching is often dependent on the sweep rate because the CDW states require time to reorder, regardless of the mechanism. In Figure 4b, we present the current versus applied in-plane electric field at different voltage sweep rates, focusing on the  $E > 30$  kV/cm range to better resolve the overlapping hysteresis region. One can see that the shapes of the hysteresis windows strongly depend on the scan rates.

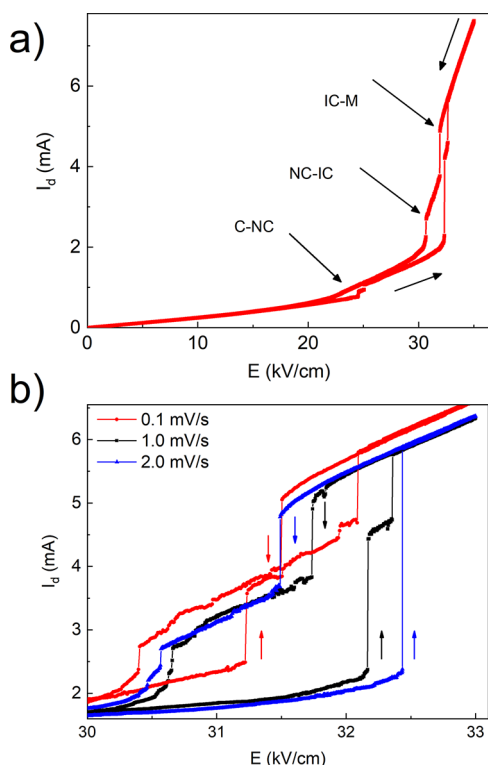
The possibility of inducing all three transitions with applied voltage bias can be further confirmed with the low-frequency noise measurements. Figure 5a shows the noise spectral density,  $S_I/I^2$ , ( $f = 10$  Hz) as a function of the applied electric field for a different device. The measurements were conducted at  $T = 77$  K to ensure that the C-CDW phase is the initial state of the device. The well-resolved peaks in the normalized noise spectral density at the field of 5 kV/cm, 8 kV/cm, and 12.5 kV/cm correspond to the C-CDW-NC-CDW, NC-CDW-I-CDW, and I-CDW-NP transitions, respectively. One can notice that the noise spectral density,  $S_I/I^2$ , is a more accurate metric of all phase transitions than the resistivity,  $R$  (see inset for comparison). It is interesting to note that the overall increase in the noise spectral density near the phase transition is often accompanied by the appearance of Lorentzian bulges in the noise frequency spectrum. In Figure 5b and c, we present the noise spectral density as a function of frequency for several values of the electric field near the C-CDW-NC-CDW and NC-CDW-I-CDW transitions. The Lorentzian in Figure



**Figure 3.** (a) Current through the device channel as a function of the applied electric field. The data were measured for the device intentionally heated to  $T = 400$  K to ensure that 1T-TaS<sub>2</sub> is in the incommensurate CDW phase. One can see a sharp increase in the current at the transition from the incommensurate CDW to normal metallic phase. (b) Normalized current noise spectral density, measured at  $f = 10$  Hz, as a function of the electric field for the same device and temperature as in panel a. The noise spectral density reveals a well-resolved peak at the transition point, marked as IC-M in the legend. (c) Normalized current noise spectral density, measured at  $f = 10$  Hz, as a function of the electric field for a different device with larger channel dimensions. The well-resolved peak in the noise spectral density, again, clearly identifies the incommensurate CDW–metallic phase transition point, marked as IC-M in the legend. The inset shows the current for this device with the distinguishable change at the transition point to the metallic phase. The data attest to the potential of the low-frequency noise spectroscopy for monitoring phase transitions in CDW materials.

$S_b$  reveals itself as a  $1/f^2$  shoulder because its central frequency is below the measurement range. The Lorentzian in Figure 5c has a central frequency  $f_0 = 30$  Hz.

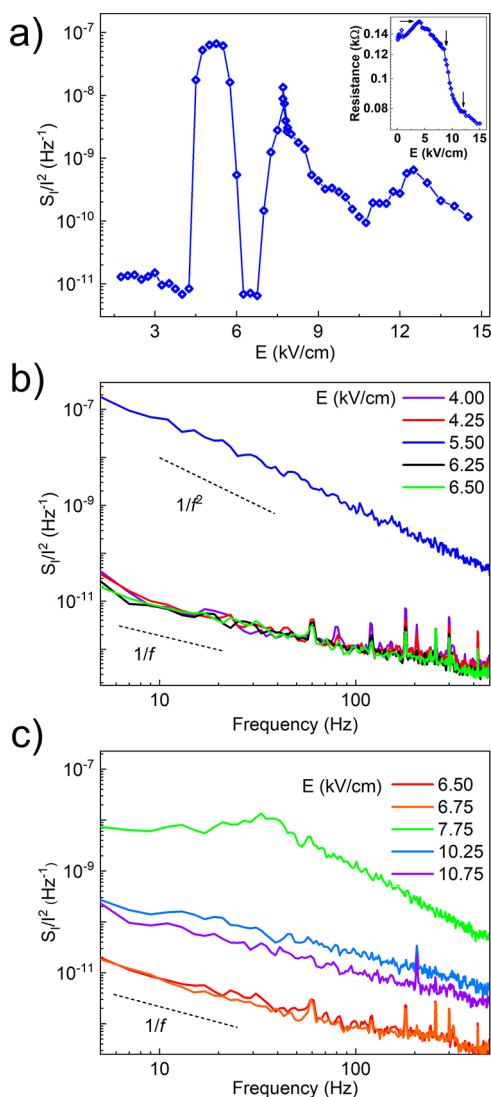
The resistance changes near the I-CDW–NP transition can vary over a large range depending on the device structure and size. Figure 6a shows the resistance in the “low-bias” regime near the I-CDW–NP transition induced by temperature. The



**Figure 4.** (a) Current through the device channel as a function of the applied bias electric field. The data were measured for the device intentionally cooled to  $T = 77$  K to ensure that 1T-TaS<sub>2</sub> is in the commensurate CDW phase. The current dependence on the field shows three consecutive hysteresis windows at  $E = 25.0$  kV/cm,  $E = 31.3$  kV/cm and  $E = 32.1$  kV/cm, which correspond to the commensurate CDW to the nearly commensurate CDW, nearly commensurate CDW to incommensurate CDW, and incommensurate CDW to metallic phases of 1T-TaS<sub>2</sub>, respectively. (b) Current through the same device measured in high-field region at different bias voltage sweep rates. The slower sweep rates allow for better resolution of the phase transitions. Note the sweep-rate dependence of the field, required to induce the transitions.

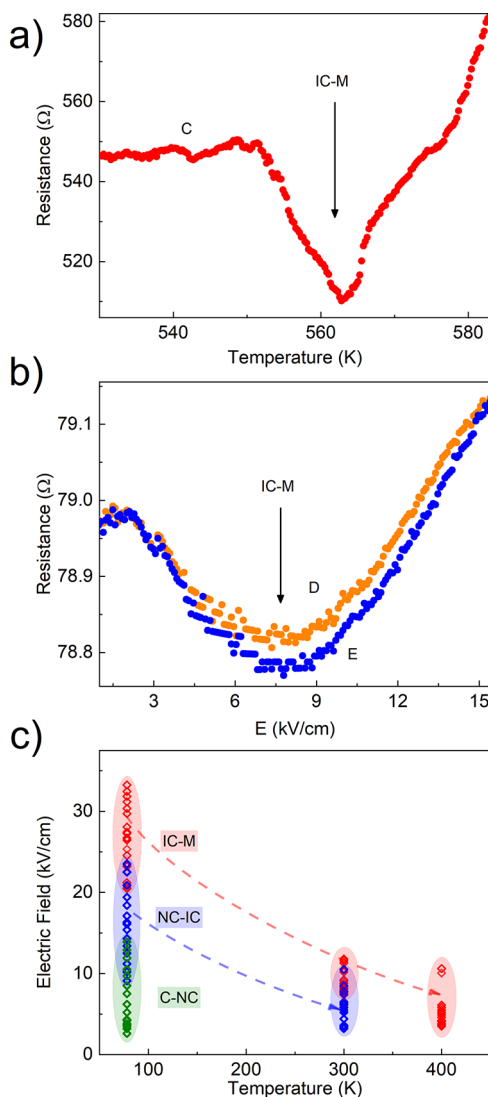
resistance changes in two other devices induced by the applied in-plane electric field are presented in Figure 6b. Utilizing a large number of 1T-TaS<sub>2</sub> devices on Si/SiO<sub>2</sub> substrate with different channel geometry and sizes, we verified that switching among three CDW and one metallic phases can be achieved in a wide temperature range. Figure 6c summarizes the results of the phase-transition switching induced by an applied electric field at different temperatures. One can see that the spread of the required electric field can be as high  $>10$  kV/cm. The electric field, that is, bias voltage, required for switching is determined by the device design and geometry, which affects the strength and distribution of electric field at a fixed bias voltage, and the dynamics of heat dissipation for a given input power. It is important to note that all the phase transitions considered here for 1T-TaS<sub>2</sub> can be induced by technologically feasible, small voltage biases. For most of the fabricated devices tested at RT, the I-CDW–NP transition was achieved at 2–3 V bias, and the bias voltage required for the NC-CDW–I-CDW phase transition was substantially lower.

We now examine the role that Joule heating of the device channel plays in the phase transitions. First, we do a simple analytical model estimate of the temperature in a representative device with the lateral dimensions,  $w \times L$ , of  $10 \mu\text{m} \times 2$



**Figure 5.** (a) Normalized current noise spectral density measured at  $f = 10$  Hz as a function of electric field applied to the device kept at 77 K. The noise spectral density reveals three well-defined peaks at the electric field of 5 kV/cm, 8 kV/cm, and 12.5 kV/cm, which correspond to the transitions from the commensurate to nearly commensurate, from the nearly commensurate to incommensurate, and from the incommensurate to normal metallic phases, respectively. The inset shows the channel resistance as a function of the electric field for the same device. The transition points are indicated with the arrows. (b) Noise spectral density as a function of frequency for several values of the electric field near the commensurate to nearly commensurate phase transition. The Lorentzian reveals itself as the  $1/f^2$  shoulder because its central frequency is below the measurement range. (c) Same as in panel b but for the electric field, which corresponds to the transition from the nearly commensurate to incommensurate phase.

$\mu\text{m}$ , and thickness  $t_f = 50$  nm ( $w$  and  $L$  are the width and length of the channel, respectively). The device structure and  $I$ - $V$  characteristics are shown in the [Supporting Information](#). At room temperature,  $T_{amb}$ , the I-CDW-NP phase transition occurs at  $V_d = 1.75$  V and  $I_d = 17.5$  mA, which corresponds to the total Joule heating power of  $P = V_d I_d = 30.6$  mW. The generated power is dissipated through the underlying  $\text{SiO}_2$  layer with a thickness of  $t_{ox} = 300$  nm and a thermal conductivity of  $k_{ox} = 1.4$   $\text{Wm}^{-1} \text{K}^{-1}$ . Although the in-plane



**Figure 6.** (a) Device channel resistance as a function of temperature near the transition from the incommensurate charge-density-wave phase to normal metallic phase. (b) Resistance as a function of applied electric field near the transition from the incommensurate charge-density-wave phase to normal metallic phase. The data are shown for two other devices with smaller geometries. (c) Summary of electric field induced phase transitions at different temperatures for 1T-TaS<sub>2</sub> devices. The variation in the electric field required to include the phase transitions is due to different device geometries, thickness of the layers in the device structures, and other variations in the device designs.

thermal conductivity of the TaS<sub>2</sub> is approximately a factor of  $\times 3$  larger than that of the SiO<sub>2</sub> layer, owing to the small cross-section of the TaS<sub>2</sub> channel,  $A_{f||} = t_f \times w$ , the total in-plane thermal resistance of the TaS<sub>2</sub> layer,  $R_{th||} = L/(k_f \times A_{f||})$  is about two orders of magnitude greater than the total cross-plane thermal resistance,  $R_{th\perp}$ , of the underlying SiO<sub>2</sub>/Si layers. For this reason, almost all dissipated heat diffuses through the SiO<sub>2</sub>/Si substrate. The total cross-plane thermal resistance is a sum of three terms,  $R_{th\perp} = R_c + R_{SiO_2} + R_{Si}$  where  $R_c$ ,  $R_{SiO_2}$ , and  $R_{Si}$  are the thermal contact resistance at the TaS<sub>2</sub>-SiO<sub>2</sub> interface, the thermal resistance of the SiO<sub>2</sub> layer, and the thermal resistance of the Si substrate, respectively. The thermal contact resistance at the interface and the thermal resistance of

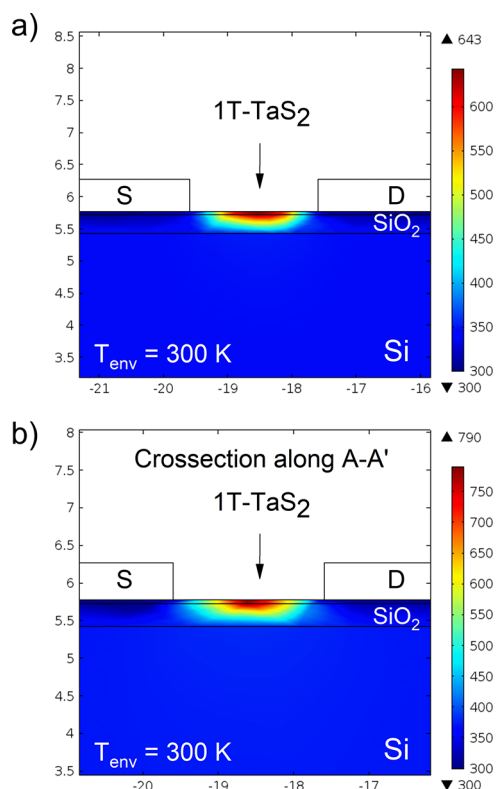
the SiO<sub>2</sub> layer are  $R_c = \{G_{int} \times A_{f,\perp}\}^{-1}$  and  $R_{SiO_2} = t_{ox}/(k_{ox} \times A_{f,\perp})$ , where  $A_{f,\perp} = w \times L$  is the device cross-plane surface area. The  $G_{int}$  (interfacial thermal conductance) values reported for typical van der Waals materials on standard substrates vary in relatively small range and mostly depend on the quality of the interface,<sup>59–63</sup> for example, 50 MW/m<sup>2</sup>K for graphene, 33 MW/m<sup>2</sup>K for WTe<sub>2</sub>, and 15 MW/m<sup>2</sup>K for MoS<sub>2</sub>, respectively. An analytical estimate of the device average temperature rise across the SiO<sub>2</sub> layer is  $\Delta T \approx P \times R_{SiO_2} \approx 328$  K, without taking into account the thermal contact resistance. This result suggests that the I-CDW–NP phase transition can take place due to the Joule heating, since the device temperature,  $T = T_{amb} + \Delta T = 628$  K, exceeds the I-CDW–NP phase transition temperature of 550 K. Inclusion of the contact resistance,  $R_c$ , will additionally heat up the device by 100–200 K, depending on the value assumed for  $G_{int}$  and the device structure.

To further understand the phase transition mechanism and separate out the temperature effect from the field effect, we have modeled the heat diffusion in the experimentally tested sample, using the finite-element method implemented in COMSOL (see [Methods](#) for details). The heat generation from Joule heating in the TaS<sub>2</sub> channel region is sensitive to the sample geometry, material properties, and ambient conditions. The effective electric field,  $E$ , and the current density,  $J$ , in the channel are taken to be same as in the experiment by tuning the sheet resistance of the TaS<sub>2</sub> active layer. The latter ensures that the Joule heating power,  $P = V_d I_d$ , corresponds to that of the experimental setup. We focus on the temperature distribution near two critical transition points: (i) just before IC-CDW–NP ( $E \sim 8.45$  kV/cm), and (ii) just after IC-CDW–NP ( $E \sim 9$  kV/cm). Since the current is localized between the inner contacts of the device structure, significant heating happens in the active region between two bias, that is, source–drain, contacts. Our simulations show that just before the phase transition, the temperature of the hotspot can rise as high as  $\sim 739$  K, well exceeding the C-CDW–NP transition temperature. After the phase transition, the temperature of the sample increases even more, up to  $\sim 864$  K. The schematic of the simulated structure and temperature rise is provided in the [Supporting Information](#).

[Figure 7a](#) and [b](#) show the temperature profile along the cross-section of the device channel (see inset to [Figure 7a](#)). The generated heat in the hotspots, indicated as red color regions at the middle of the channel, dissipates mainly through the SiO<sub>2</sub> layer and Si substrate. Owing to its low thermal conductivity, the SiO<sub>2</sub> layer acts as an effective thermal barrier, and prevents effective heat dissipation to the Si substrate. The latter results in substantial heating, which drives the phase transitions. The obtained numerical data for the specific device geometry are in agreement with the analytical estimate above. The radiation loss from the top surface becomes important at elevated temperature. However, it is not significant enough to change the conclusion that Joule heating is the reason behind the C-CDW–NP phase transition in TaS<sub>2</sub> devices of the considered geometry, on SiO<sub>2</sub>/Si substrate.

## CONCLUSIONS

We investigated the bias-voltage driven switching among three charge density wave phases, commensurate, nearly commensurate, incommensurate, and the normal metallic phase in thin films of 1T-TaS<sub>2</sub> induced by an in-plane electric field. The switching among all four phases has been achieved, which is a



**Figure 7.** (a) Simulated temperature distribution profile along the cross-section of the device channel for the voltage bias just before the C-CDW–NP transition. The hot spot temperature exceeds 550 K, which is above the C-CDW–NP transition. (b) Same as in panel a but for the voltage bias, which corresponds to the regime above the C-CDW–NP phase transition. The temperature increases owing to the lower resistance of 1T-TaS<sub>2</sub> in the metallic NP, which results in stronger Joule heating.

key prerequisite for nanoscale device applications. We have demonstrated that an application of a small bias voltage to a device kept at room temperature can induce the transition from the nearly commensurate and incommensurate phases to the normal metallic phase. The low-frequency electronic noise spectroscopy was used as an effective characterization tool for monitoring the transitions, particularly the switching from the incommensurate charge-density-wave to the normal phase. The noise spectral density experiences sharp increases at the phase transition points, which correspond to the step-like changes in resistivity. The assignment of the phases has been confirmed by the low-field resistivity measurements over the temperature range from 77 to 600 K. Analysis of the experimental data and simulations of heat dissipation indicates that self-heating plays a dominant role in the electric-field induced transitions. Furthermore, the results demonstrate the potential of the noise spectroscopy for investigating phase transitions in low-dimensional charge density wave materials.

## METHODS

**Preparation of 1T-TaS<sub>2</sub> Crystals by CVT.** Briefly, tantalum (20.4 mmol, Sigma-Aldrich 99.99% purity), sulfur (41.1 mmol, J.T. Baker >99.9% purity), and iodine (J.T. Baker 99.9% purity,  $\sim 88$  mg for an ampule with a  $\sim 14.0$  cm<sup>3</sup> volume) were added to a  $\sim 18 \times 1$  cm<sup>2</sup> cleaned, dried, fused quartz ampule. After evacuation, filling with Ar, and sealing, the ampule was heated in a two-zone tube furnace at  $10$  °C min<sup>−1</sup> to  $975$ – $875$  °C (hot–cold gradient) for 1 week. The 1T-

TaS<sub>2</sub> polymorph was isolated as golden, multimillimeter-sized crystals by quenching the hot ampule in a water–ice–NaCl bath.

**Device Fabrication.** We utilized the shadow mask method to directly deposit TLM structures onto preselected 1T-TaS<sub>2</sub> thin films obtained by mechanical exfoliation. The exfoliated layers of 50–60 nm were relatively stable in the air, which allowed us to use the shadow mask method.<sup>64</sup> The method allowed us to avoid the damage from chemical contamination, typically associated with conventional lithographic lift-off processes. It also drastically reduced the total air exposure time and the fabrication process. It takes less than an hour to fabricate a device by the shadow mask method, compared to 2–3 days required for the standard lithography process. The designed shadow masks of TLM configuration were fabricated using the double-side polished Si wafers with 3 μm thermally grown SiO<sub>2</sub> on both sides (Ultrasil Corp.; 500 μm thickness of P-type; <100>). The shadow mask fabrication process began with evaporation of 200 nm thick chromium (Cr) film on the front side of the wafer, followed by a combination of electron beam lithography (EBL) and Cr etchant (1020A) to create TLM pattern. This was followed by the fluorine-based reactive ion etching (RIE) to transfer the pattern to the underlying SiO<sub>2</sub>. Finally, the pattern was transferred into the underlying Si substrate using the deep reactive ion etching (DRIE) (Oxford Cobra). Since the 500 μm thick Si wafer is too bulky to etch through from the top, a large window was opened at the back side of the wafer by photolithography to remove the bulk Si until a thin Si membrane is left. Finally, the DRIE etch step was timed to break through the thin silicon membrane and release the stencil from the top. The shadow masks were directly used to fabricate plenty of devices by aligning them with preselected flakes on the device substrate using an optical microscopy, clamping the aligned mask and device substrate together, and placing the clamped assembly in an electron beam evaporator (EBE) for contact deposition (10 nm Ti and 100 nm Au) through the mask openings. The completed devices were then transferred to another vacuum chamber for electrical characterization. The thickness and width of 1T-TaS<sub>2</sub> flakes were determined using atomic force microscopy (AFM) and scanning electron microscopy (SEM) inspection.

**Electronic Noise Measurements.** The noise spectra were measured with a dynamic signal analyzer (Stanford Research 785). To minimize the 60 Hz noise and its harmonics, we used a battery biasing circuit to apply voltage bias to the devices. The devices were connected to Lakeshore cryogenic probe station TTPX. All *I*–*V* characteristics were measured in the cryogenic probe station (Lakeshore TTPX) with a semiconductor analyzer (Agilent B1500). The noise measurements were conducted in the two-terminal device configuration but with different channel length to determine the contribution of contact noise. Since the contact resistances of the devices are very low, the extracted contact noise was lower than thermal noise and lower than thermal noise and had no significant contribution to the noise due to the channel. The dynamic signal analyzer measures the absolute voltage noise spectral density *S<sub>V</sub>* of a parallel resistance network of a load resistor, *R<sub>L</sub>* (3.6 kΩ), and device under test (DUT), *R<sub>D</sub>*. The normalized current noise spectral density, *S<sub>I</sub>/I<sup>2</sup>*, is calculated from the equation: *S<sub>I</sub>/I<sup>2</sup>* = *S<sub>V</sub>* × [(*R<sub>L</sub>* + *R<sub>D</sub>*)/(*R<sub>L</sub>* × *R<sub>D</sub>*)]<sup>2</sup>/(*I*<sup>2</sup> × *G*<sup>2</sup>), where *G* is the amplification of the low-noise amplifier (1000).

**Finite Element Simulations.** To model the heat distribution in the TaS<sub>2</sub> channel, we used the finite element model, implemented in COMSOL Multiphysics package.<sup>65</sup> The simulated device geometry corresponds to an experimental sample, which has a 50 nm thick TaS<sub>2</sub> sample on top of a 4 μm thick Silicon substrate. Four 2.5 μm × 10 μm Au electrodes are placed on top of TaS<sub>2</sub>, with intercontact separations of 2 μm. Bias is applied between the two middle Au contacts. In the experiment, the C–CDW–NP transition happens for *V* = 1.69 V (19.25 mA) and 1.80 V (24.58 mA). The same electrical conditions are maintained in the simulation geometry. In case of thermal conduction, heat dissipation can be described by standard heat equation,

$$\rho C_p \frac{dT}{dt} = \nabla(\kappa \nabla T) + q_e \quad (2)$$

where  $\rho$  is the mass density,  $C_p$  is the heat capacity,  $T$  is temperature, and  $\kappa$  is thermal conductivity. The left side of eq 2 will disappear under steady state condition. On the right side of eq 2, Joule heating is captured by the generation term,  $q_e = J \times E = \sigma |VV|^2$ , where  $J$  is the current density,  $E$  is the electric field,  $\sigma$  is the electrical conductivity, and  $V$  is the applied bias. The generated heat will appear as an outward heat flux, giving rise to a thermal gradient,  $\nabla T$ . The electrical conductivity of the TaS<sub>2</sub> channel ( $\sigma$ ) is tuned to match the current and power density of the experimental sample. The thermal conductivity of TaS<sub>2</sub> ( $\kappa$ ) is around 4–10 Wm<sup>-1</sup> K<sup>-1</sup>.<sup>66</sup> For SiO<sub>2</sub> layer, the thermal conductivity is 1.4 Wm<sup>-1</sup> K<sup>-1</sup>.<sup>67</sup> The metal contacts, as well as the bottom face of the Si substrate, are assumed to be always at room temperature (300 K). Radiating heat boundary conditions are applied on the exposed TaS<sub>2</sub> and SiO<sub>2</sub> surfaces as,  $\hat{n} \cdot \kappa \nabla T = \epsilon \sigma (T_{env}^4 - T^4)$ , where  $T_{env}$  is the ambient temperature (300 K),  $\hat{n}$  is the surface normal, and  $\epsilon$  is the emissivity (0.8). All other surfaces are assumed to be thermally insulating ( $\hat{n} \cdot \kappa \nabla T = 0$ ).<sup>68</sup>

## ASSOCIATED CONTENT

### Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.9b02870.

SEM/EDS, PXRD, and Raman characterization of 1T-TaS<sub>2</sub> crystals, atomic force microscopy images and height profile of representative 1T-TaS<sub>2</sub> devices, high-field current–voltage characteristics, normalized noise spectral density and simulated temperature distributions in 1T-TaS<sub>2</sub> devices on a SiO<sub>2</sub>/Si substrate (PDF)

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### Author Contributions

A.A.B. conceived the idea, coordinated the project, contributed to experimental data analysis, and led the manuscript preparation; A.G. fabricated the devices, conducted current–voltage and noise measurements, and contributed to data analysis; S.R. supervised noise measurements and contributed to data analysis; B.D. conducted simulations and contributed to data analysis; F.K. contributed to analysis of experimental and simulation data and performed analytical derivations; A.N. tested high-temperature current–voltage characteristics; R.K.L. supervised numerical simulations and contributed to data analysis; M.B. supervised high-temperature measurements. M.B. synthesized 1T-TaS<sub>2</sub> crystals and conducted materials characterization; T.T.S. supervised material synthesis and contributed to materials characterization. All authors contributed to writing the manuscript.

### Notes

The authors declare no competing financial interest.

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